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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,389	02/25/2004	Frankie F. Roohparvar	400.007US02	2908
7590	10/04/2004		EXAMINER	
Andrew C. Walseth Leffert Jay & Polglaze, P.A. P.O. Box 581009 Minneapolis, MN 55458-1009			PEIKARI, BEHZAD	
			ART UNIT	PAPER NUMBER
			2186	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/786,389	ROOHPARVAR, FRANKIE F.
	Examiner	Art Unit
	B. James Peikari	2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 25 February 2004.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-11 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 25 February 2004 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>2/25/04</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____ .

DETAILED ACTION

Specification

1. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 7 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter that was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

There is nothing in the specification that teaches the plurality of addressable banks comprising only four blocks.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-6 and 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schumann et al., U.S. 5,732,017, in view of Lee, 5,307,314.

Schumann et al. teach a multi-bank, synchronous, non-volatile memory made up of an array of memory cells (*note Figure 1, Flash memory 11 and EEPROM 13*), with associated write latches (*note Figure 1, latches 39, 23 and 24*) to latch at data and an associated processor to transfer data to and from the Flash banks using read/write circuitry (*note Figure 1, at least elements 15, 17, 19, 25, 27, 29, 31, 32, 34, 35, and 37*) coupled to the memory array, wherein data may be read out of one bank while data is written into another bank (*Note Figure 1 and the explanation thereof, especially column 3, lines 66-67*).

Although Schumann et al. do not explicitly teach the use of more than one processor accessing the multi-bank system described above, it was well known that multiprocessing systems provided a significant speed and performance advantage over uniprocessor systems, although at a greater cost. Memories having plural banks that allowed simultaneous accesses to occur were particularly well suited to multiprocessor environments because, for example, a dual bank memory allowing simultaneous access to two banks would have been functionally equivalent to two separate smaller memories, each simultaneously able to allow access one of two processors. In fact, this advantage was plainly stated by Lee et al. (*note at least column 5, lines 17-26*). Consequently, it would have been obvious for one having ordinary skill in the art at the time the invention was made to incorporate multi-bank memory of Schumann et al. into

a multiprocessor environment such as that described by Lee et al., to allow simultaneous memory access by both processors, since this would have been both faster and more efficient, for at least the reasons described above.

6. Claims 1-6 and 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pashley et al., U.S. 6,418,506, in view of Lee, 5,307,314.

Pashley et al. teach a multi-bank, synchronous, non-volatile memory made up of an array of memory cells (*Note Figure 2, Flash array 203*), with associated write buffering (*Note Figure 2, buffer 202 and buffer 208*) to latch at data and an associated processor (200) to transfer data to and from the Flash banks using read/write circuitry (*note Figure 2, at least elements 201, 204, 205, 206, 207, 208, 209, and 210*) coupled to the memory array, wherein data may be read out of one bank while data is written into another bank (*Note Figure 2 and column 4, lines 50 et seq.*)

Although Pashley et al. do not explicitly teach the use of more than one processor accessing the multi-bank system described above, it was well known that multiprocessing systems provided a significant speed and performance advantage over uniprocessor systems, although at a greater cost. Memories having plural banks that allowed simultaneous accesses to occur were particularly well suited to multiprocessor environments because, for example, a dual bank memory allowing simultaneous access to two banks would have been functionally equivalent to two separate smaller memories, each simultaneously able to allow access one of two processors. In fact, this advantage was plainly stated by Lee et al. (*note at least column 5, lines 17-26*).

Consequently, it would have been obvious for one having ordinary skill in the art at the time the invention was made to incorporate multi-bank memory of Pashley et al. into a multiprocessor environment such as that described by Lee et al., to allow simultaneous memory access by both processors, since this would have been both faster and more efficient, for at least the reasons described above.

7. Claims 1-6 and 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akaogi et al., U.S. 6,240,040 B1, in view of Lee, 5,307,314.

Akaogi et al. teach a multi-bank, synchronous, non-volatile memory made up of an array of memory cells (*note Figure 1, banks 202, 204, 206 and 208*), with associated write buffering (*Note Figure 1, elements 220, 224 and 228*) to latch at data and an associated processor to transfer data to and from the Flash banks using read/write circuitry (*Note Figure 1, at least elements 218, 210, 212, 214, and 216*) coupled to the memory array, wherein data may be read out of one bank while data is written into another bank (*Note the Abstract, Figure 1 and column 4, lines 52 et seq.*)

Although Akaogi et al. do not explicitly teach the use of more than one processor accessing the multi-bank system described above, it was well known that multiprocessor systems provided a significant speed and performance advantage over uniprocessor systems, although at a greater cost. Memories having plural banks that allowed simultaneous accesses to occur were particularly well suited to multiprocessor environments because, for example, a dual bank memory allowing simultaneous access to two banks would have been functionally equivalent to two separate smaller

memories, each simultaneously able to allow access one of two processors. In fact, this advantage was plainly stated by Lee et al. (*note at least column 5, lines 17-26*). Consequently, it would have been obvious for one having ordinary skill in the art at the time the invention was made to incorporate multi-bank memory of Akaogi et al. into a multiprocessor environment such as that described by Lee et al., to allow simultaneous memory access by both processors, since this would have been both faster and more efficient, for at least the reasons described above.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 1-6 and 8-11 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-15 and 28-38 of copending Application No. 09/627,770. Although the conflicting claims are not identical, they are not patentably distinct from each other because every feature of

the claims of the present invention which was either explicitly taught or would have been obvious in view of limitations of claims 1-15 and 28-38 of the copending application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (703) 305-3824. The examiner is generally available between 8:00 am and 9:30 pm, EST, Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 746-7239 (Official communications)

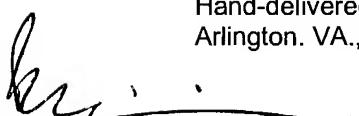
or:

(703) 746-7240 (for Informal or Draft communications)

or:

(703) 746-7238 (for After-Final communications)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,
Arlington, VA., Sixth Floor (Receptionist).



B. James Peikari
Primary Examiner
Art Unit 2186

September 27, 2004